A Review of:

Digital-Pixel Focal Plane Array Technology

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Who It's Meant For:

This paper is meant to show off the work that Lincoln Labs has done to develop digital focal plane array technology. At a company like Lincoln Labs the general principal is "Publish or Perish". The paper is meant to show the potential for this technology and to use their recent technological breakthroughs to secure future funding. That being said, this technology has the potential to revolutionize IR/EO and Lidar imaging systems and therefore should be funded. The resolution, SNR and dynamic range capabilities of digital focal plane array are unmatched by any current sensor systems.

Recent Development of Digital Focal Plane Arrays:

Recently MIT has developed a 250-megapixel long-wave infrared imaging system that uses a 256x256 digital-pixel focal plane array (DFPA). The sensor system combines a commercially produced detector array with a digital-pixel readout integrated circuit (DROIC) which enables it to be adapted to existing systems. A prototype sensor system using the DFPA has already been developed and field tested. An LWIR image recorded by the sensor system can be seen in Figure 1 below:

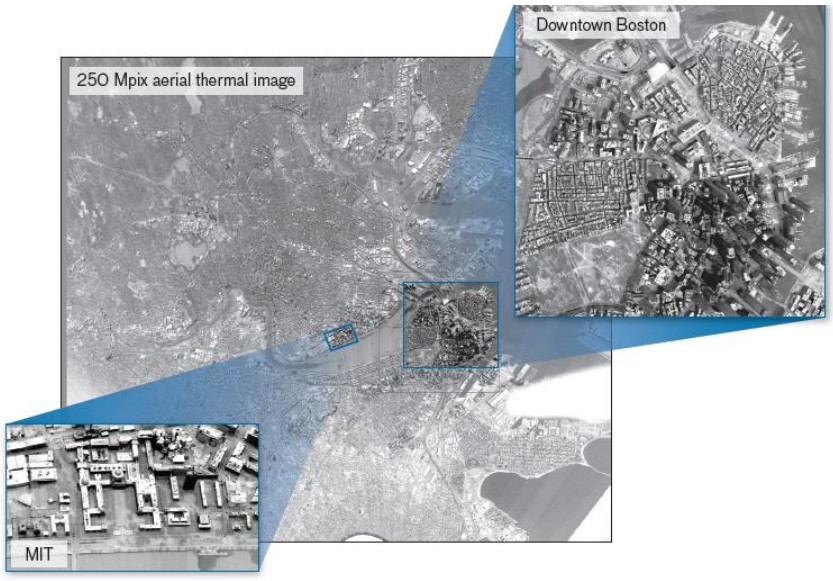

Figure 1: LWIR image of the Boston area using MIT's DFPA. The MIT inset in the lower left-hand corner corresponds to approximately a 1-megapixel image.

Conventional Focal Plane Array Technology:

The focal plane array (FPA) is the heart of most modern day infrared imaging systems. Its job is to convert an optical image into an electrical signal that can be read out and processed. To achieve maximum sensitivity the FPA is integrated into an evacuated dewar and cryogenically cooled to minimize thermally generated currents. As light strikes the FPA a photocurrent is generated and stored in a capacitor (electron well). An example circuit diagram for the FPA can be seen in Figure 2 below. Typically, a low noise amplifier (M_i) is used to isolate the photodetector bias from the rest of the unit cell circuit. Two switches are also used to control the multiplexor readout and to drain the storage capacitor. In (c) it is seen that the storage capacitor occupies the majority of the unit cell area. That is because this capacitor (aka the unit cell well depth) determines the maximum sensitivity of the FPA. The maximum signal to noise ratio is achieved when:

$$SNR_{max} = \frac{Signal_{max}}{Noise} = \frac{N_{well}}{\sqrt{N_{well}}} = \sqrt{N_{well}}$$

Where $Signal_{max}$ represents the maximum measureable signal in units of photoelectrons, *Noise* represents the Poisson-process-limited statistical variation, and N_{well} is the well depth in units of photoelectrons. A well depth of 25 million photoelectrons (typical for a very good FPA) results in a maximum shot-noise-limited SNR of ~5000.

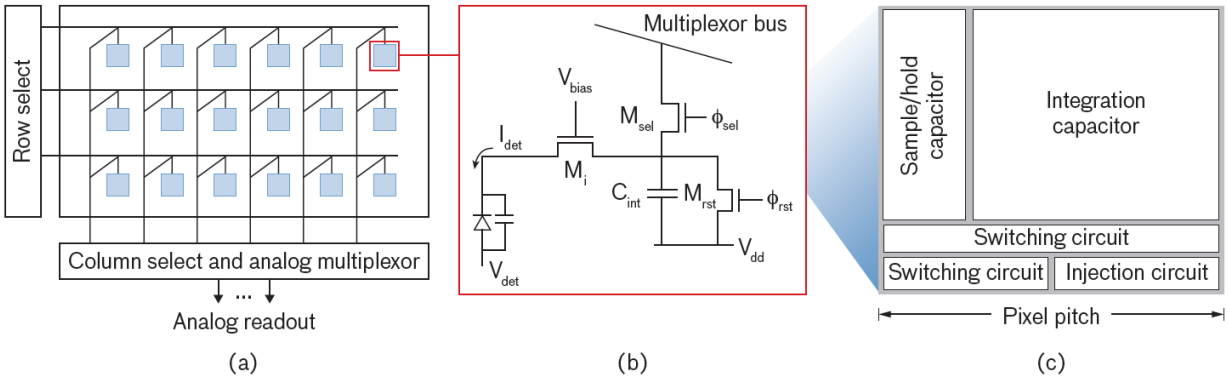

Figure 2: (a) FPA architecture with (b) simplified unit cell circuit diagram and (c) unit cell layout.

Digital Focal Plane Array Technology:

The Digital Focal Plane Array developed at MIT overcomes the limitations of traditional FPAs by performing in-pixel signal digitization. By doing this it enables larger dynamic range, faster low-noise all digital readout and on-chip processing. An example unit cell can be seen in Figure 3 below. The circuit consists of a bias buffer amplifier (similar to the FPA), an in pixel analog-to-digital converter, a storage capacitor, a multiplexor to connect the counter/shift register to one of four nearest neighbor unit cells and pixel timing and control circuits. As with the FPA the photocurrent is stored in a capacitor. When the capacitor fills (voltage reaches a preset threshold) a comparator circuit is tripped. The output of the comparator is fed to (1) a circuit that resets the voltage across the capacitor and (2) a pulse generation circuit that is input to an N-bit digital counter. So, the photocurrent (light on detector) is proportional to how fast the capacitor fills and resets which determines the frequency of the pulse waveform and the output of the digital counter. Since the capacitor is allowed to reset it can be much smaller which buys room for the added digital circuitry. These capacitors typically fill at about 6000 photoelectrons - compared to 25 million in a FPA. When used with a 16-bit digital counter the system saturates at approximately 230million photoelectrons – 10x that of a FPA.

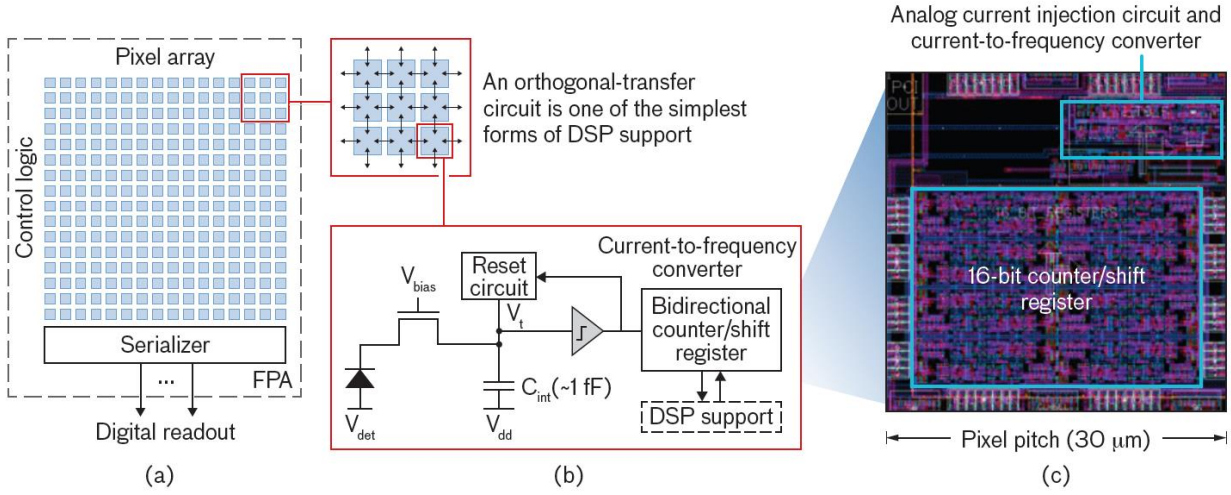

Figure 3: (a) DFPA architecture with (b) simplified unit cell circuit diagram and (c) unit cell layout.

Advantages of Going Digital:

One of the major advantages of the digital focal plane array is its ability for ultra-sensitive imaging. Since it effectively has a well depth of 10x that of a FPA it has a higher dynamic range and SNR. Under ideal (shot-noise-limited) conditions the increased well depth translates to a factor of over 2.5 improvement in SNR (shown in Figure 4). The SNR and dynamic range can be further increases by suppressing low frequency noise and calibrating the detector to subtract off a known background estimate.

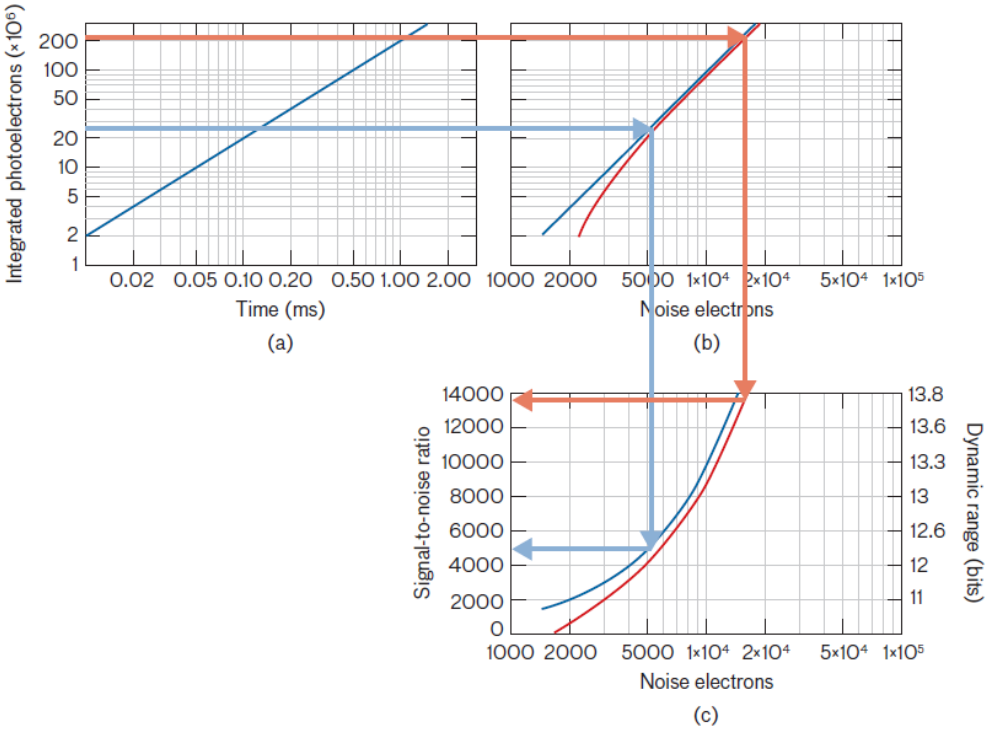

Figure 4: A DFPA (orange) with a well depth of 230million photoelectrons can produce a SNR of ~13,500 when operated in shot noise limited conditions. A FPA (blue) with a well depth of 25million photoelectrons produces a SNR of ~5000 when operated in shot noise limited conditions.

Other advantages consist of electronic on-chip Image stabilization – which takes advantage of the high speed orthogonal transfer of the digital signals, ultra-large pixel count infrared imagery, on chip filtering – both spatial and temporal, and image wide lock in amplification.

Potential Future Development of Digital Focal Plane Arrays:

Lincoln Labs has fabricated DROIC devices using IBM 90nm and 65nm low-power digital integrated circuit process that enables up to ~2000 transistors in be integrated within a single digital unit cell (~100x that of a FPA). As technology continues to advance these transistors will get smaller and higher density CMOS fabrication processes can be used to increase in-unit cell processing capacity. Figure 5, suggests how this increases transistor density anticipated in the next decade will impact the in-pixel signal processing capabilities.

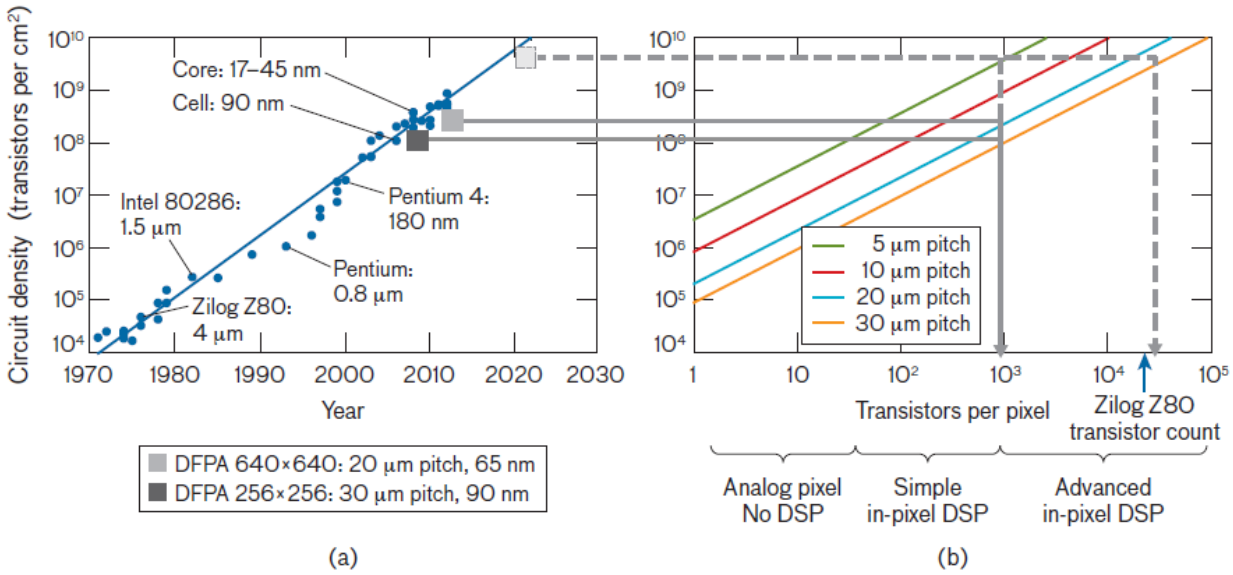

Figure 5: (a) The circuit transistor density and trend line for state of the art commercial microprocessors plotted versus the year each microprocessor was introduced to the marketplace. (b) The maximum number of transistors that can be packed into a pixel unit cell for several pixel sizes

Further improvements (shown in Table 1) include improved manufacturing processes, larger format arrays, smaller pixels, higher bit counters, increased wavelength capabilities, faster data transfer and improved in-pixel computation. It is clear that digital focal plane arrays will push the boundaries of future applications including day/night persistent surveillance, border patrol and protection, aerial search and rescue, environmental remote sensing as well as military imaging and targeting.

Table 1. Digital-Pixel Readout Integration Circuit Parameters		
DROIC FEATURES	**CURRENT**	**FUTURE**
Manufacturing process	65–90 nm	≤32 nm
Format	256 × 256 640 × 480	1280 × 720 4028 × 4028
Pitch	20 µm 30 µm	≤12 µm
Bits	14–21	>28
Digital count	~3000–6000 electrons	<100 electrons
Wavelength	SWIR–LWIR	Visible-VLWIR
Data rate	Up to 32 Gbps	100 Gbps
Orthogonal transfer	Yes	Yes
In-pixel computation	• Up-down counter – Background subtraction – Spatial filtering • Split counter – 2-kernel spatial filtering – In-phase and quadrature AC signal detection – Compressive sensing – Multifunction sensing	• Multiple independently controllable counters – Temporal matched filtering • Threshold detection logic