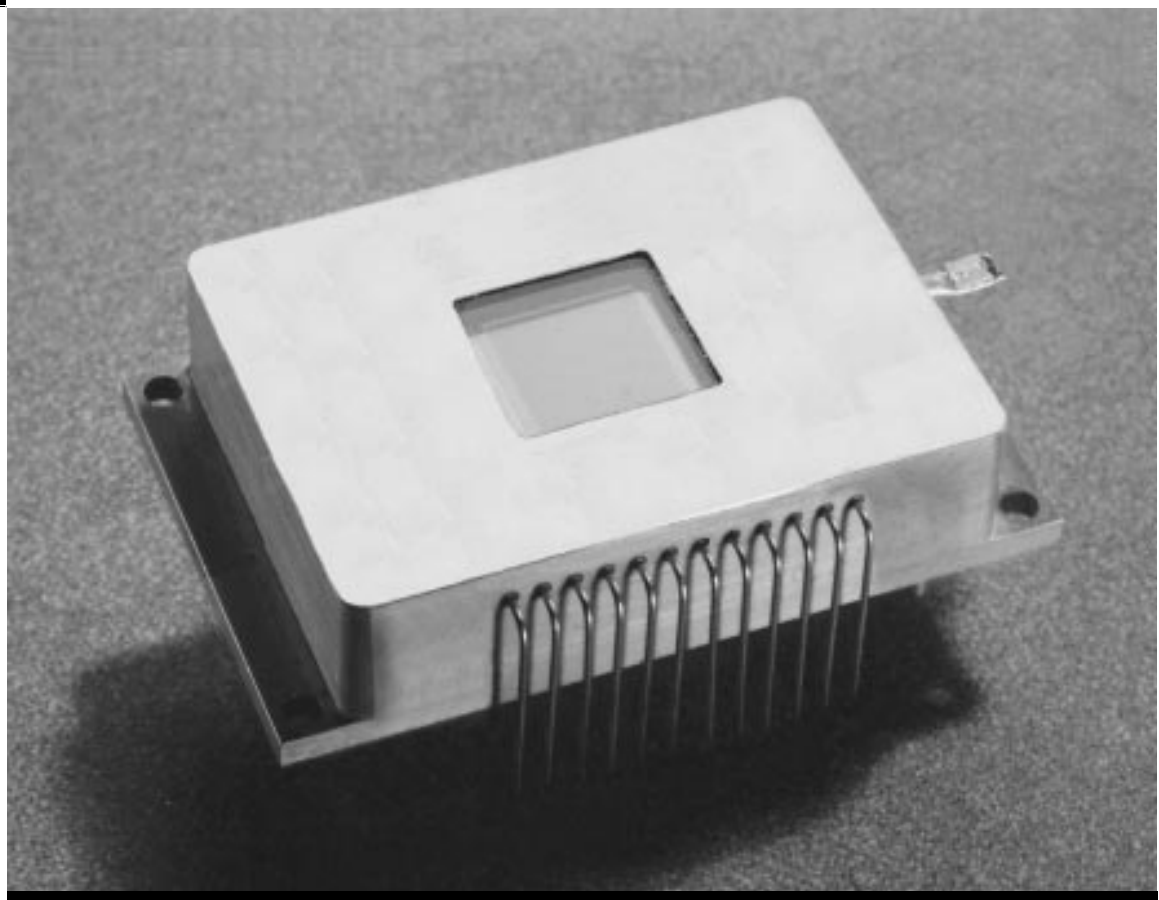

PRELIMINARY

SITe 512 x 512 Thermoelectrically Cooled Scientific-Grade CCD

- 512 x 512 pixel format (24μm square)
- Front-illuminated or thinned, back-illuminated versions
- Packaged with a two stage Thermoelectric cooler for improved performance without a dewar
- Unique thinning and Quantum Efficiency enhancement processes
- Excellent QE from IR to UV
- Anti-reflection coating for visible region
- MPP technology
- Low dark current
- Excellent charge transfer efficiency (CTE) at all signal levels
- On-chip output MOSFET for low noise
- Wide dynamic range
- Applications include astronomy, machine vision, medical imaging, X-ray imaging, and scientific imaging

SIA502A CCD Imager: *Ideal for applications with small-area imaging and very low dark current requirements*

General Description

The SIA502A CCD Imager is a silicon charge-coupled device designed to efficiently image scenes at low light levels from UV to near infrared. The sensor is fabricated as a 512 x 512 pixel, full frame area imager that utilizes a buried channel, three level polysilicon gate process. Features include a buried channel with a mini-channel for high transfer efficiency, multi-phase pinned (MPP) operation for low dark current, and a lightly doped drain (LDD) amplifier for low read noise. The device is available in a front illuminated version or a thinned, back-illuminated version that provides superior quantum efficiency.

The CCD is thermoelectrically (TE) cooled using a two stage cooler that is an integral part of the package. The sealed vacuum package prevents the device from collecting moisture when it is cooled below dew point temperature and prevents thermal conduction of heat to the device. SITe's unique thinning and back surface enhancement process provides increased blue and UV response in a flat and fully supported die.

Thermoelectric Cooler

The two stage thermoelectric cooler mounted inside the sealed vacuum package can maintain the CCD at a temperature of approximately 65 to 70 degrees C lower than the external temperature of the heat sink. The external heat sink must be properly cooled for this to be accomplished. The dark current of the CCD is a strong function of temperature. It will increase by a factor of two for every 7ºC of temperature increase. By maintaining the CCD at -35ºC, the dark current will be reduced to >200X less than its room temperature value. This is a significant reduction and worth the extra circuitry and cooling provisions needed to remove the heat from the heat sink. Since the thermoelectric cooler itself generates heat during the cooling process, the heat being removed at the heat sink is greater than the heat removed from the CCD.

Functional Description

Imaging Area

As shown in the functional diagram, Figure 4, the imaging area of the SIA502A consists of 512 columns, each of which contains 512 picture elements (pixels). Each pixel measures 24µm x 24µm. The columns are isolated from each other by channel-stop regions. There is an output amplifier at each end of the two output serial registers. Only one output is used for the SIA502A. The unused upper serial register is biased off to prevent its dark current from leaking into the image array

The signal charge collected in the imaging array is transferred along the columns, one row at a time, to the serial output register and from there to the output amplifier.

Three levels of polysilicon are used to fabricate the three gate electrodes which form the basic CCD cell (pixel). All of the pixels in a given row are defined by the same three gates. Corresponding gates in each row within a group of 512 are connected in parallel at both edges of the array. The clock signals used to drive the imaging area gates are brought in from both edges of the array, thus increasing the rate at which the rows can be shifted.

Serial Registers

The functional diagram (Figure 4) illustrates the relationship between the imaging array and the serial registers. The upper serial register is not used and is biased off. The charge collected in the imaging section is transferred through the transfer gate into the lower serial register phase 1 gate. The serial output register has one pixel for each column in the imaging array, plus 15 extra pixels at the end for a total of 527. The extra pixels serve as a dark reference and ensure the signal chain stabilization when the image data is received at the output.

The output of the serial register is terminated in a summing well, a DC-biased last gate (which serves to decouple the serial clock pulses from the output node), and an output amplifier. The summing well is a separately clocked gate equal in charge capacity to the other serial gates. Noiseless charge summing of consecutive serial pixels. is possible using this gate. Similarly, it is possible to sum pixels into the serial register by performing repetitive parallel transfers with the serial clocks fixed. In this manner, it is possible to collect and detect as one pixel the sum of the charge in sub-arrays of the imaging section. The sum of this sub-array charge must be less than the full well charge. The well capacity of a pixel in the serial register is greater than that of a parallel pixel to ensure that the charge handling capacity is large enough for this summing operation.

Output Structure

The imager has a single output MOSFET that is located at the end of the extended serial register. Figure 1 presents a schematic diagram of the output configuration. The output amplifier reset gate (RG), reset drain (RD), summing well (SW), and last gate (LG) are brought out to individual pins. This allows the operational voltages for the output to be optimized.

A positive pulse is applied to the reset gate (RG). This resets the potential of the floating diffusion to the potential connected to the reset transistor drain (RD). The reset gate voltage is then turned off and the output node (the floating diffusion) is isolated from the rest of the circuit. The charge from the serial pixel is then transferred to the output node on the falling edge of the summing well (SW) clock signal. The addition of charge on the output node causes a change in the voltage on the gate of the output MOSFET. This change in voltage is sensed at OUT.

Timing

The SITe SIA502A CCD Imager has one operating output (OUT). The device operates in the full frame mode with the entire imager's signal transferring to the one output. This timing is shown in Figure 6. The same numbered phases of the serial register are internally connected and clocked together. Likewise, all the same numbered

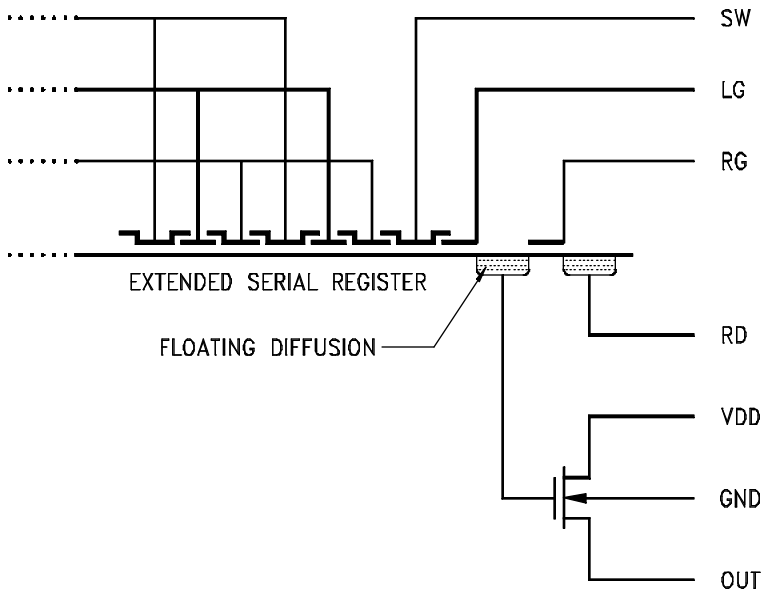

FIGURE 1 *Output Structure*

phases of the parallel registers are internally connected and clocked together.

The transfer gate (TG) adjacent to the serial output register must be clocked. The upper transfer gate next to the unused serial register should be held low to prevent unwanted charge in this register from entering the parallel registers. The unused serial register's gates are not clocked.

Timing diagrams for the single output are shown in Figure 5. During a parallel or serial shift, the signal charge is transferred one pixel at a time. A frame readout consists of at least 512 parallel shift and serial readout sequences for a full frame. Figure 4 shows the typical timing for a full frame readout. A serial readout sequence consists of at least 527 serial shifts for full frame mode (15 for each serial extended region plus 512 pixels of data from the imaging array). The serials are static when the parallels are shifting and vice-versa. During integration, the serial clock is normally kept running continuously to flush the serial register and to stabilize the bias levels in the off-chip signal chain.

The timing diagrams (Figures 5 and 6) are for integration under phases 1 and 2. For MPP operation, this timing is a requirement (as it is with all SITe MPP devices). For reference, typical timing for the clamp and sample signal of an external charge detection circuit are included in the output timing diagrams.

Multi-Phase Pinned (MPP) Operation

The multi-phase pinned (MPP) technology used on the SIA502A allows the device to be operated totally inverted during integration and line readout. The main advantage of this mode of operation is that it results in much lower dark current than conventional CCD operation. Other advantages of MPP operation are the reduction of surface residual image defect and a greater tolerance for ionizing radiation environments. To operate the CCD in the MPP mode, the array clocks are biased sufficiently negative to invert the n-buried channel and "pin" the surface potential beneath each phase to the substrate potential. This allows holes from the p+ channel stop to populate the surface states at the silicon/silicon dioxide interface, minimizing surface dark current generation.

To enable all three phases of the array to be inverted and still retain well capacity, MPP devices have an extra implant under the phase 3 gates. During integration, this creates a potential barrier between each pixel allowing signal charge to accumulate under phases 1 and 2 at each pixel site. A consequence of this mode of operation is that the total well capacity is about 50 percent of that of a standard CCD if all the parallel clocks are operated at the same voltages. A larger well capacity can be obtained if phase 3 parallel clock high rail is operated about 3 volts higher than the phase 1 and phase 2 high rails.

DEVICE SPECIFICATIONS

Measured at -45 deg. C, unless otherwise indicated, 45 kpixels/sec and standard voltages using a dual slope CDS circuit (8 µs integration time)

	Minimum	*Typical*	*Maximum*
Format		512 x 512 pixels	
Pixel Size		24 µm x 24 µm	
Imaging Area		12.3 mm x 12.3 mm	
Dark current (MPP), *20°C equivalent*		50 pa/cm^2	70 pa/cm^2
Readout noise Front		5 electrons	7 electrons
Back		7 electrons	9 electrons
Full Well signal	300,000 electrons	350,000 electrons	
Output gain	1.0 µV/ electron	1.5 µV/ electron	
CTE per pixel	0.99995	0.99999	
Storage Temperature	-20		+60
Temperature Sensor		Analog Devices, AD590	

TE COOLER SPECIFICATIONS

(Assumes 5mW of optical energy on the CCD array.)

Parameter	*Minimum*	*Typical*	*Maximum*
Heat Sink Power Load (watts)		19	26
Voltage (volts)		12	
Current (amps)		1.5	2
CCD Temperature (°C)	-45	-35	
Heat Sink Temperature (°C)		35	

TABLE 1 *Device specifications, SIA502A*

DC OPERATING CONDITIONS

TERMINAL	ITEM	MIN	STANDARD	MAX	UNIT
BIAS1	BIAS VOLTAGE1 (UNUSED SERIAL)	12	14	16	V
BIAS2	BIAS VOLTAGE2 (UNUSED SERIAL GATES)		0		V
VDD	OUTPUT DRAIN SUPPLY	20	23	25	V
RD	RESET DRAIN	12	14	16	V
LG	LAST GATE	-4	-2	0	V
SUB	SUBSTRATE CONNECTION		0		V
ID	INPUT DIODE SUPPLY	5	15	23	V
TG2	TRANSFER GATE (UNUSED SERIAL)	-10	-9	0	V
OUT	MOSFET OUTPUT (LOAD)	5	15	50	kohms

GATE TO SUBSTRATE VOLTAGES

TERMINAL	ITEM		MIN	STANDARD	MAX	P TO P MAX	UNIT
RG	RESET GATE	LOW RAIL	-5	0	5	20	V
		HIGH RAIL	5	12	15		V
S#	SERIAL GATE	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V
SW	SUMMING WELL	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V
P#	PARALLEL GATE	LOW RAIL	-10	-9	0	20	V
		HIGH RAIL	0	4	10		V
P3		HIGH RAIL	0	7	10		V
TG1	TRANSFER GATE	LOW RAIL	-10	-9	0	20	V
		HIGH RAIL	0	7	10		V
SG	SAMPLE GATE	LOW RAIL	-10	-4	0	20	V
		HIGH RAIL	5	8	15		V

TABLE 2 SIA502A *DC operating conditions and clock voltages*

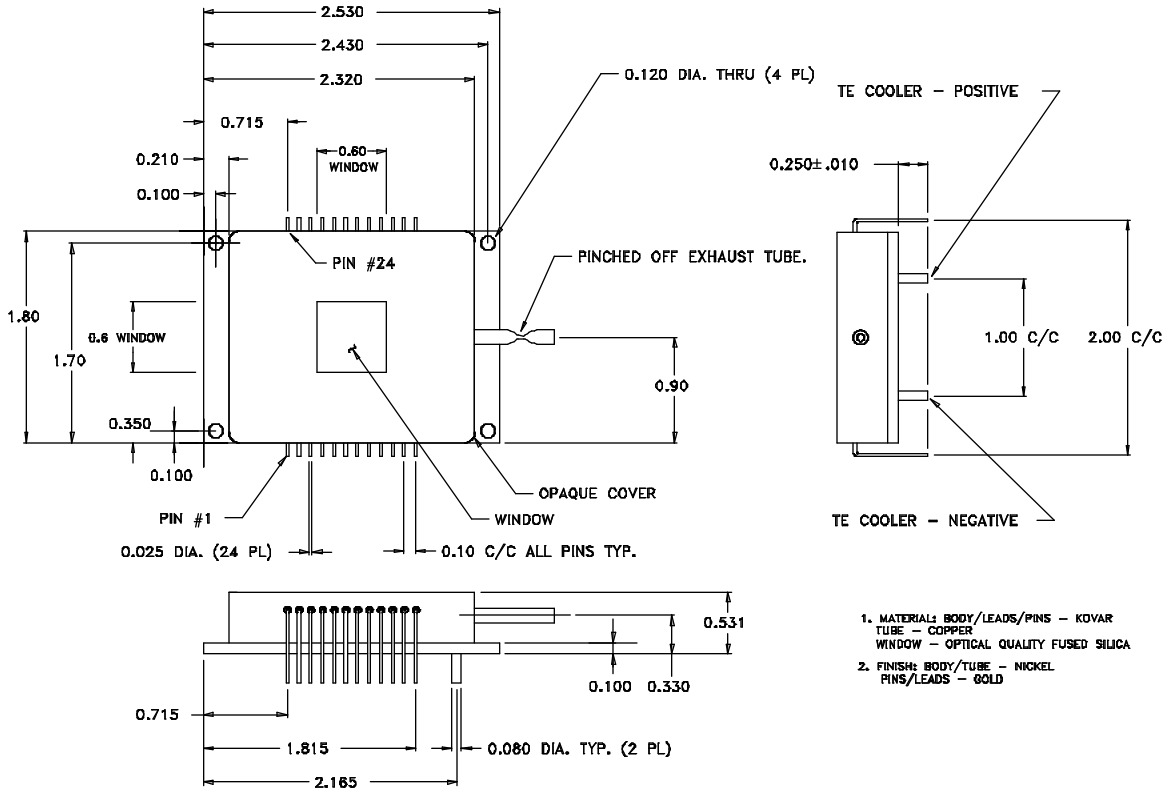

FIGURE 2 SIA502A *package configuration*

SIA502A PIN DEFINITION			
PIN #	**FUNCTION**	**REGISTERS**	**SYMBOL**
1	Substrate Ground	all registers	SUB
2	Input Diode, serial output register	serial output register	ID
3	Sample gate, Input to serial output register	serial output register	SG
4	Serial phase 3	serial output register	S3
5	Serial phase 2	serial output register	S2
6	Serial phase 1	serial output register	S1
7	Summing well	serial output register	SW
8	Last gate	serial output register	LG
9	Reset transistor gate	serial output register	RG
10	Reset Drain	serial output register	RD
11	Output transistor drain	serial output register	VDD
12	Output transistor source	serial output register	OUT
13	No Connection		N/C
14	No Connection		N/C
15	No Connection		N/C
16	Bias 2, unused serial register gates	unused serial register	BIAS2
17	Bias 1, VDD,RD,RG of unused serial register output	unused serial register	BIAS1
18	Temperature Sensor Diode - Negative		TSD (-)
19	Temperature Sensor Diode - Positive		TSD (+)
20	Transfer gate 2, unused upper serial register	unused serial register	TG2
21	Parallel phase 3	all parallel registers	P3
22	Parallel phase 1	all parallel registers	P1
23	Parallel phase 2	all parallel registers	P2
24	Transfer gate 1, serial output register	serial output register	TG1
BOTTOM	TEC POWER SUPPLY		TEC(+)
BOTTOM	TEC POWER SUPPLY		TEC(-)

TABLE 3 *pin definitions*

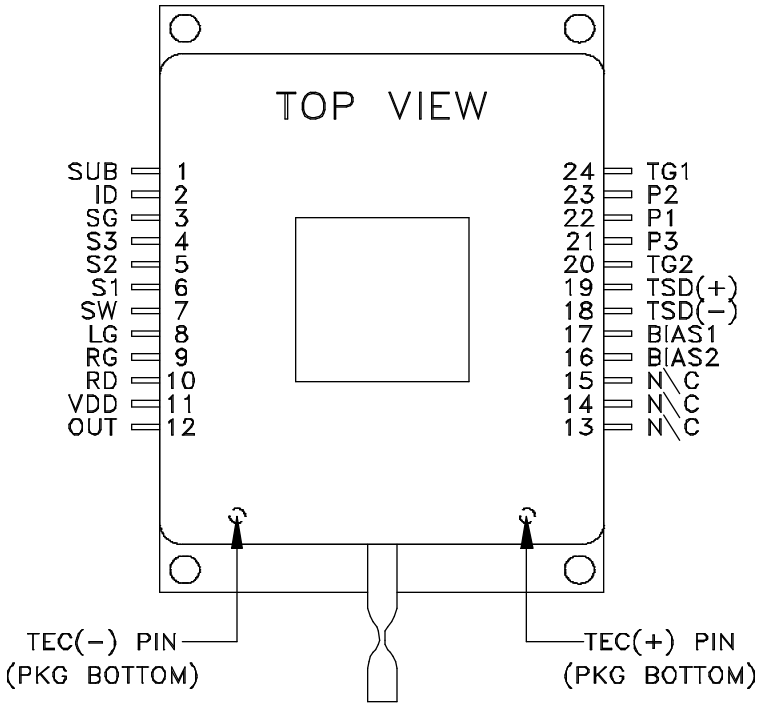

FIGURE 3 SIA502A *pin labels*

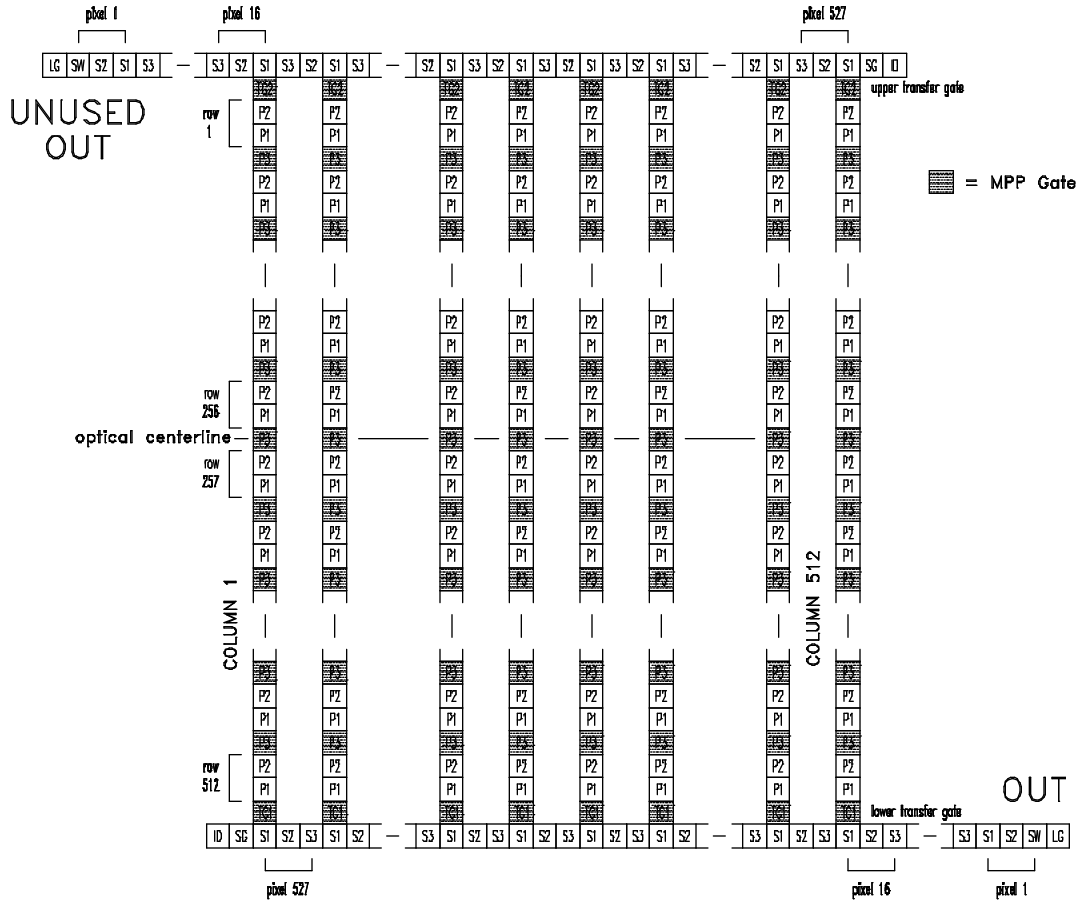

FIGURE 4 SIA502A *functional diagram*

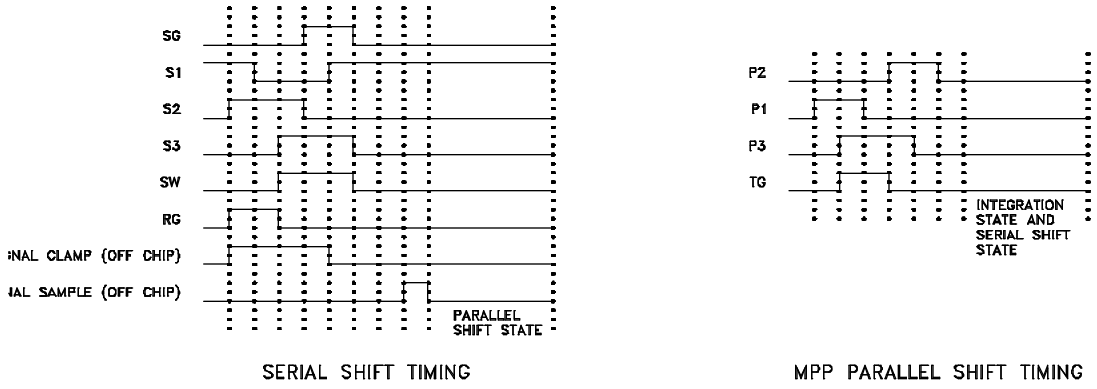

FIGURE 5 *Serial and Parallel timing*

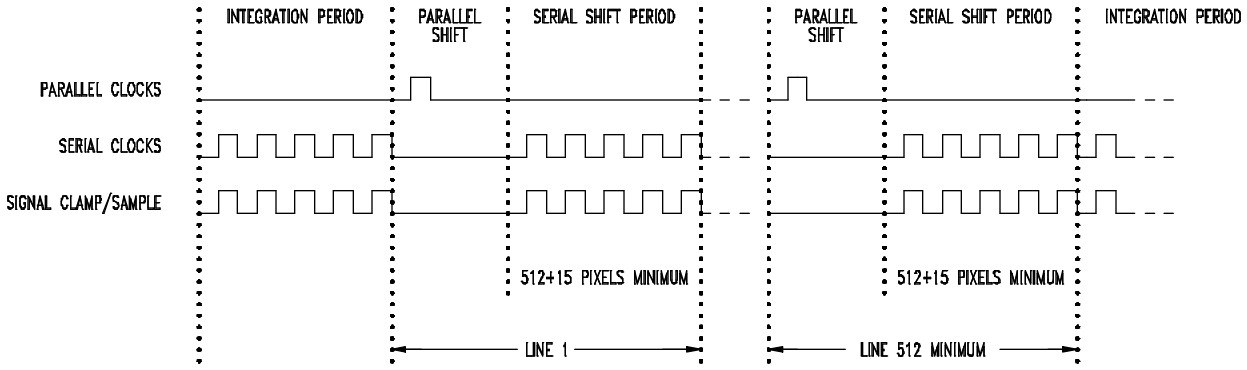

FIGURE 6 *Typical full-frame readout*

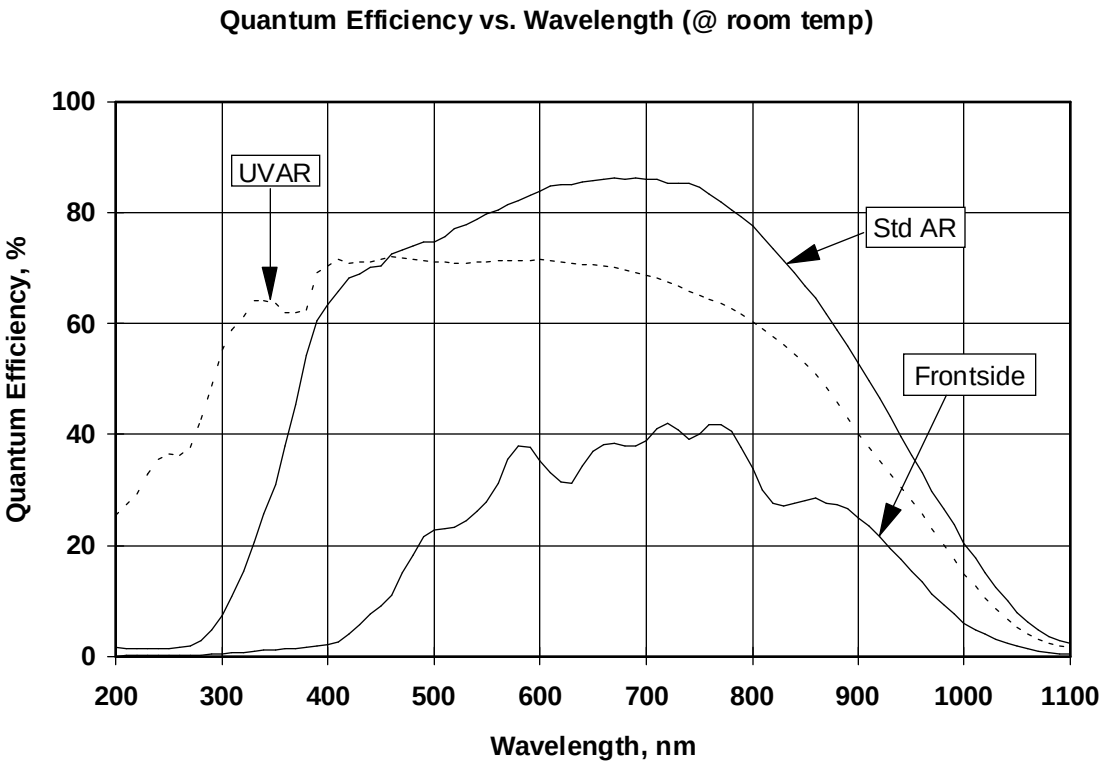

FIGURE 7 *Typical QE curves*

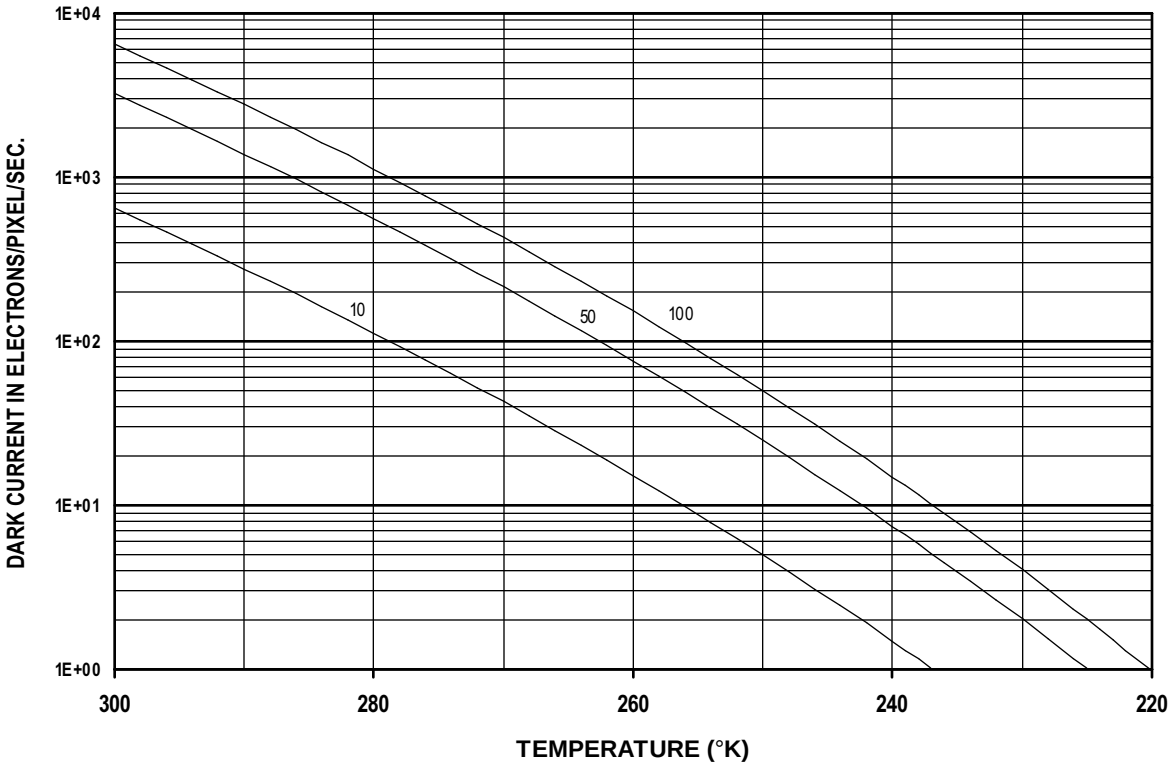

FIGURE 8 *Effect of temperature on dark current. Parameter is pAmp/cm^2 at 293K*

SCIENTIFIC IMAGING TECHNOLOGIES, INC.

P.O. Box 569
Beaverton, Oregon 97075-0569
503/644-0688
503/644-0798 fax

Scientific Imaging Technologies, Inc. (SITe) specializes in the research, design, and manufacture of charge-coupled devices (CCDs) and imaging subassemblies containing CCD components. SITe's scientific grade CCDs are used in applications for astronomy, aerospace, medical, military surveillance, spectroscopy, and other areas of imaging research. Commercial uses of SITe high performance CCDs include such areas as biomedical imaging, manufacturing quality control, environmental monitoring, and nondestructive testing.

With its focus on scientific-grade CCD imaging components and modules, SITe provides standard designs, user defined custom CCDs, and foundry services. SITe's engineering and manufacturing team builds custom CCD imagers for use in the most demanding applications including NASA programs, satellite platforms, and other research projects. Device formats are available as front illuminated or thinned, back illuminated CCDs.

Innovation, process development, and design experience date back to the founding of the group in 1974.

Product Precautions

Scientific Imaging Technologies, Inc. (SITe) realizes the use of charge-coupled devices (CCDs) for imaging is rapidly expanding into new applications. Awareness of the sensitivity of CCDs to electrostatic discharge (ESD) damage and the steps that can be implemented to prevent damage are very important to the end user.

With the exception of the back-illuminated SI424A, SITe imagers do not have built-in gate protection structures. Even with the protection structures, the imagers are very sensitive to ESD damage. It is imperative that proper precautions be taken whenever the imagers are handled.

The damage caused by ESD can be immediate and fatal (hard damage) resulting in a completely nonfunctional device. ESD damage can also be more subtle with no immediate device performance degradation. In this case, the result is a slow deterioration (soft damage) that may not be apparent until after extended operation.

There are three major areas where special procedures are required. We recommend that our customers use these procedures to minimize the risk of ESD damage.

1. Work areas specifically designed to minimize ESD.

2. Personnel requirements for ESD damage protection.

3. Use special ESD protected handling and shipping containers. SITe has developed a custom shipping container which grounds all the CCD pins together and allows clean and safe handling for incoming inspection and storage.

For more specific information on minimizing ESD damage, refer to SITe's technical briefing called "Recommended ESD Handling Procedures For CCD Imagers."

SITe Lit. No. SIA502A
revision date: 12/20/95